
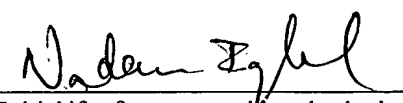


FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)					Attorney Docket Number 5347-210		Serial No. not yet assigned	
					Applicants: Ronald DeShawn Blanton			
					Filing Date concurrently herewith			Group
U. S. PATENT DOCUMENTS								
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
N1	1.	5,546,408	8/13/96	Keller	371	27	JC929 U.S. PTO 09/866357  05/25/01	
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation Yes No	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
N1	2.	K. Dwarakanath et al; <i>Universal Fault Simulation Using Fault Tuples</i> ; Annual ACM IEEE Design Automation Conference; Proceedings of the 37 th conference on Design automation; June 5-9, 2000, Los Angeles, CA USA pp 786-789.						
N1	3.	Rao Desineni et al; <i>Universal Test Generation Using Fault Tuples</i> ; ITC International Test Conference (31 st : 2000: Atlantic City, NJ) Proceedings International Test Conference 2000: October 3-5, 200, New Atlantic City Convention Center, Atlantic City, NJ, USA; pp 812-819.						
N1	4.	TestBench, Library Data Reference, Ninth Edition; Version 2000, IBM Corporation; Endicott, NY 13760; pp 170-181 and 177-183.						
N1	5.	M. Abramovici et al; <i>Digital Systems Testing and Testable Design</i> ; IEEE Press; The Institute of Electrical and Electronics Engineers, Inc., New York; pp 292-294 and 197-199.						
N1	6.	J. Khare et al; <i>Fault Characterization of Standard Cell Libraries Using Inductive Contamination Analysis (ICA)</i> 14 th VLSI Test Symposium - 1996 pp 405-413.						

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N1	7.	S. Gai et al; <i>MOZART: A Concurrent Multilevel Simulator</i> ; IEEE Transactions on Computer Aided Design, Vol. 7, No. 9, September 1988; pp 1005-1016.	
N1	8.	Scott Davidson; <i>ITC '99 Benchmark Circuits - Preliminary Results</i> ; Sun Microsystems, Inc., ITC International Test Conference; Paper P6.0 (1125), 1999.	
	9.	S. Ma et al; <i>An Experimental Chip to Evaluate Test Techniques Experiment Results</i> ; Center for Reliable Computing; International Test Conference; Paper 28.3 (663-672), 1995.	
	10.	J. Paul Roth; <i>Diagnosis of Automata Failures: A Calculus and a Method</i> ; IBM Journal, July 1966, pp 278-291.	
	11.	F. Brglez; <i>Accelerated ATPG and Fault Grading Via Testability Analysis</i> ; Proceedings of ISCAS 1985 IEEE pp 695-698..	
	12.	G. Smith; <i>Model for Delay Faults Based Upon Paths</i> ; 1985 International Test Conference; Paper 9.6 (342-349).	
	13.	K. Butler; <i>The Stuck-at Fault: It Ain't Over 'Til It's Over</i> ; International Test Conference; Paper P10.1 (1165), 1998, IEEE.	
	14.	Y. Gong et al; <i>Locating Bridging Faults Using Dynamically Computed Stuck-At Fault Dictionaries</i> ; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17. No. 9, September 1998; pp 876-887.	
	15.	M. Gharaybeh et al; <i>Classification and Test Generation for Path-Delay Faults Using Single Stuck-Fault Tests</i> ; International Test Conference; Paper 5.4 (139-148), IEEE, 1995.	
	16.	J. Patel; <i>Stuck-at Fault: A Fault Model for the Next Millennium</i> ; University of Illinois at Urbana-Champaign; International Test Conference; Paper P10.2 (1166), IEEE, 1998.	
	17.	W. Chen et al; <i>Test Generation in VLSI Circuits for Crosstalk Noise</i> ; Department of Electrical Engineering-Systems; International Test Conference; Paper 25.3 (641-650).	
	18.	K. Lee et al; <i>Test Generation for Crosstalk Effects in VLSI Circuits</i> ; IEEE (1996) pp 628-631.	
	19.	W. Kautz ; <i>Testing for Faults in Combinational Cellular Logic Arrays</i> ; Stanford Research Institute; Proceedings of the 8 th Symposium on Switching Automation Theory, pp 161-174, 1967.	
	20.	H. Al-Asaad et al; <i>ESIM: A Multimodel Design Error and Fault Simulator for Logic Circuits</i> ; IEEE (April 2000), Proceedings of the 18 th VLSI Test Symposium, pp 221-228.	
N1	21.	J. Roth et al; <i>Programmed Algorithms to Compute Tests to Detect and Distinguish Between Failures in Logic Circuits</i> ; IEEE Transactions on Electronic Computers, Vol. EC-16, No. 5, October 1967; pp 71-83.	
N1	22.	H. Lee et al; <i>HOPE: An Efficient Parallel Fault Simulator for Synchronous Sequential Circuits</i> ; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15. No. 9, September 1996; pp 1048-1058.	
N1	23.	P. Banerjee et al; <i>Characterization and Testing of Physical Failures in MOS Logic Circuits</i> ; IEEE Design & Test (August 1984); pp 76-86.	
N1	24.	R.D. Blanton et al; <i>Properties of the Input Pattern Fault Model</i> ; IEEE 1997; pp 372-380.	

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N1	25.	P. Nigh et al; <i>An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, IDDq and Delay-fault Testing</i> ; IEEE 1997; pp 459-464.	
N1	26.	F. Ferguson et al; <i>Extraction and Simulation of Realistic CMOS Faults using Inductive Fault Analysis</i> ; 1988 International Test Conference; Paper 25.1; pp 475-484.	
N1	27.	H. Lee et al; <i>Soprano: An Efficient Automatic Test Pattern Generator for Stuck-Open Faults in CMOS Combinational Circuits</i> ; 27 th ACM/IEEE Design Automation Conference; Paper 39.2; 1990; pp 660-666.	
N1	28.	U. Mahlstedt et al; <i>Simulation of non-classical Faults on the Gate Level - The Fault Simulator COMSIM</i> ; International Test Conference; pp 883-892, October 1993.	
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N1	30.	R.L. Wadsack; <i>Fault Modeling and Logic Simulation of CMOS and mos Integrated Circuits</i> ; The Bell System Technical Journal, May-June 1978 pp 1449-1473.	
N1	31.	S. Ma et al; <i>An Experimental Chip to Evaluate Test Techniques Experiment Results</i> ; International Test Conference; Paper 28.3, IEEE 1995 pp 663-672.	

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